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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/265,119	03/09/1999	MAURIZIO PERI	856063.579	4151

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	16

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/265,119	Applicant(s) PERI ET AL.	
	Examiner Ayal I Sharon	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10-13,16-22 and 24* is/are rejected.

7)☒ Claim(s) *6,14-15 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-24 of U.S. Application 09/265,119 were filed on 03/09/1999, with a Foreign Priority filing date of 9/30/98. A Request for Reconsideration, Declaration, and IDS (papers #11-13) were filed on 3/27/2003. Amendment A (paper #9) was filed on 11/7/2002. Claim 9 was cancelled in the amendment, and Claim 8 was amended. Amendment B (paper #15) was filed on 9/18/2003. Claims 1 and 5 were amended, and new claims 21-24 were added in Amendment B.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Interpretations

3. In paper #7, Examiner interpreted a "Flash" memory structure as being a "flash EEPROM" as described in Brigati et al., U.S. Patent 6,011,717, Col. 1, lines 24-31. Examiner also interpreted "Flash EPROM" as being a set of devices that include "flash EEPROM".

4. In paper #9, p.14, the Applicants requested that "the pending claims ... be 'given the broadest reasonable interpretation consistent with the specification.'" As mandated by MPEP §2113.

5. Examiner is providing the following definitions in order to clarify the definitions of the terms.

   - According to the Lee '923 et al., U.S. Patent 5,777,923 (col. 1, lines 13-19):

     > "In essence, a flash memory is an electrically erasable programmable read only memories (EEPROM) that supports three operations: read, program and erase."

   - According to the Lee '923 et al., U.S. Patent 5,777,923 (col. 1, lines 49-54):

     > "Known flash memories have several drawbacks. Some known flash memories perform block program and erase functions to initialize the entire memory into a predetermined state prior to programming the memory with new data. There is no flexibility to select arbitrary words or bits within a block to be efficiently erased or programmed. An example is given in Table 1."

   Therefore, Examiner interprets the difference between EEPROM and Flash to be that Flash can only be erased one block at a time, whereas EEPROM enables smaller element sizes to be erased.

6. Applicants note in paper #15, p.8, that "the term of art used for the smallest block that can be erased in a FLASH memory is the term "sector". Examiner agrees with the Applicants that thses definitions are substantially the same.

Claim Objections

7. Claim 24 is objected to because of the following informalities: "comprising ... **few** memory cells than ...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 contains the following typographical error, which renders the claim indefinite: "... memory cells Flash memory cells being emulated."

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. The prior art used for these rejections is as follows:

- Hasburn et al., U.S. Patent 5,682,497. (Henceforth referred to as "**Robinson '497**").

12. **Claims 10-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Robinson '497.**

13. In regards to Claim 10, Robinson '497 teaches the following limitations:

> 10. A Flash memory device for emulating an EEPROM, comprising:

first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and
(Robinson '497, especially: col.1, lines 22-47; col.2, line 46 to col.3, line 32; Fig.3 and col.5, line 50 to col.6, line 64; col.15, line 20 to col.18, line 65)

a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and
(Robinson '497, especially: Figs.5-8 and col.7, line 65 to col.9, line 4)

a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.
(Robinson '497, especially: Fig.1, Items 28-34 and col.4, line 18 to col.col.5, line 50; col.15, line 20 to col.18, line 65)

14. In regards to Claim 11, Robinson '497 teaches the following limitations:

11. The Flash memory device of claim 10 wherein the first and second Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second Flash memory portion.
(Robinson '497, especially: Figs.3-8 and col.5, line 51 to col.9, line 4)

15. In regards to Claim 12, Robinson '497 teaches the following limitations:

12. The Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.
(Robinson '497, especially: Figs.3-8 and col.5, line 51 to col.9, line 4)

16. In regards to Claim 13, Robinson '497 teaches the following limitations:

13. The Flash memory device of claim 12 wherein the plurality of Flash memory portions include two Flash memory portions, each with four memory blocks, each memory block including 64 memory pages each with 16 memory locations that are able to store a data byte.
(Robinson '497, especially: col.5, lines 50-51;)

Figs.9-12 each show 8 memory storage locations. The use of 16 instead of 8 is a matter of design choice.

17. In regards to Claim 16, Robinson '497 teaches the following limitations:

> 16. A method of emulating an EEPROM using Flash memory, the method comprising:
>
> dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)
>
> assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors;
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)
>
> in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)
>
> in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

18. In regards to Claim 17, Robinson '497 teaches the following limitations:

> 17. The method of claim 16, further comprising, in response to a third write instruction to write to the selected page address when a most recent write instruction to write to the selected page address was executed by writing to a last memory block of the first memory sector, executing the third write instruction by writing to a first memory block of the second memory sector.
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

19. In regards to Claim 18, Robinson '497 teaches the following limitations:

> 18. The method of claim 16 wherein all memory pages sharing a same page address constitute a set of memory pages, the number of sets of memory pages equaling how many memory pages are in each memory block, the method further comprising:
> (Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)
>
> assigning to each set of memory pages of the first and second memory sectors a page pointer that reflects which memory page in the set has been most recently updated; and

(Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

in response to each write instruction requesting to write data to the selected page address, determining which page pointer is associated with the selected page address, determining from the page pointer associated with the selected page address which memory page of the set of memory pages assigned the selected page address is next to be updated, and writing the data in the memory page that is determined to be the next memory page to be updated.
(Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

20. In regards to Claim 19, Robinson '497 teaches the following limitations:

19. The method of claim 16, further comprising erasing the second memory sector while updating memory pages of the first memory sector.
(Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

21. In regards to Claim 20, Robinson '497 teaches the following limitations:

20. The method of claim 19 wherein the erasing act is performed in plural erase phases, with each of the erase phases being triggered by writing data in the first memory sector.
(Robinson '497, especially: col.15, line 20 to col.18, line 65; Figs.3-8 and col.5, line 51 to col.9, line 4)

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The prior art used for these rejections is as follows:

- Lee, U.S. Patent 5,956,268. (Henceforth referred to as "**Lee '268**").
- James et al., U.S. Patent 5,966,723. (Henceforth referred to as "**James**")

24. Claims 1-5, 7-8, 21-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee '268 in view of James.

25. In regards to Claim 1, Lee '268 teaches the following limitations:

> 1. An emulated EEPROM memory device,
> (Lee '268, especially: col.2, line 47 – col.3, line 33)
>
> the memory macrocell including a Flash memory structure formed by a predetermined number of sectors, at least one sector of the Flash memory structure having a selected number of EEPROM memory cells, the selected number of EEPROM being fewer than the selected number of memory cells Flash memory cells being emulated.
> (Lee '268, especially: col.3, line 62 – col.4, line 5)

However, Lee '268 does not expressly teach the following limitations:

> comprising a memory
> macrocell which is embedded into an integrated circuit having a microcontroller,

James, on the other hand, does teach these limitations (see col.3, line 64 – col.4, line 22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee '268 with those of James, because James (col.3, lines 22-30) expressly states that "A non-volatile device having a serial interface is described. Although the detailed description describes embodiments based on a flash memory device, the invention may be used in any non-volatile semiconductor memory, including, but not limited to EPROMs, EEPROMs, and flash memories, and including technologies such as NOR, NAND, AND, Divided bit-line (DINOR) and Ferro-electric random access memory (FRAM)." Lee '268 (see Abstract) teaches a "... novel nonvolatile Flash EEPROM array [that] preferably comprises a plurality of blocks which comprise a plurality of sectors of NOR-gate transistors."

26. In regards to Claim 2, Lee '268 teaches the following limitations:

> 2. The emulated EEPROM memory device according to claim 1, wherein said EEPROM byte alterability is emulated by hardware means,
> (Lee '268, especially: col.2, line 47 – col.3, line 33)

27. In regards to Claim 3, Lee '268 teaches the following limitations:

> 3. The emulated EEPROM memory device according to claim 1, wherein 8 Kbyte of the Flash memory structure are used to emulate 1 Kbyte of an EEPROM memory portion
> (Lee '268, especially: col.3, line 62 – col.4, line 5)

28. In regards to Claim 4, Lee '268 teaches the following limitations:

> 4. The emulated EEPROM memory device according to claim 1, wherein first and second EEPROM emulated sectors are each divided in a pre-determined number of blocks of the same size and each block is divided in pages.
> (Lee '268, especially: col.3, line 62 – col.4, line 5; col.5, line 64- col.6, line 7)

29. In regards to Claim 5, Lee '268 does not expressly teach the following limitations.

James, however, does teach these limitations:

> 5. The emulated EEPROM memory device according to claim 2,
>
> wherein hardware means include a state machine for controlling an address counter which is output connected to an internal address bus running inside the memory macrocell,
> (James, especially: Fig.2, Item 21; col.5, lines 10 - col.6, line 12)
>
> said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update.
> (James, especially: Fig.2, Items 6 and 27 "To Address Counter"; col.4, line 60 to col.5, line 10)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee '268 with those of James, because James (col.3, lines 22-30) expressly states that "A non-volatile device having a serial interface is described. Although the detailed description describes embodiments based on a flash memory device, the invention may be used in any

non-volatile semiconductor memory, including, but not limited to EPROMs, EEPROMs, and flash memories, and including technologies such as NOR, NAND, AND, Divided bit-line (DINOR) and Ferro-electric random access memory (FRAM)." Lee '268 (see Abstract) teaches a "... novel nonvolatile Flash EEPROM array [that] preferably comprises a plurality of blocks which comprise a plurality of sectors of NOR-gate transistors."

30. In regards to Claim 7, Lee '268 does not expressly teach the following limitations. James, however, does teach these limitations:

> 7. The emulated EEPROM memory device according to claim 1, wherein Flash and EEPROM memories operations are controlled through a register interface mapped into the memory.
> (James, especially: Fig.2, Items 3,5,6,7,9; col.4, lines 4-14)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee '268 with those of James, because James (col.3, lines 22-30) expressly states that "A non-volatile device having a serial interface is described. Although the detailed description describes embodiments based on a flash memory device, the invention may be used in any non-volatile semiconductor memory, including, but not limited to EPROMs, EEPROMs, and flash memories, and including technologies such as NOR, NAND, AND, Divided bit-line (DINOR) and Ferro-electric random access memory (FRAM)." Lee '268 (see Abstract) teaches a "... novel nonvolatile Flash EEPROM array [that] preferably comprises a plurality of blocks which comprise a plurality of sectors of NOR-gate transistors."

31. In regards to Claim 8, Lee '268 teaches the following limitations:

comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability
(Lee '268, especially: col.3, line 62 –col.4, line 5)

by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages
(Lee '268, especially: col.5, line 65 –col.6, line 7)

Lee '268 does not expressly teach the following limitations. James, however, does teach these limitations:

8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors,
(James, especially: Fig.2, Item 9)

and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode.
(James, especially: col.5, lines 10 - col.6, line 12)

wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector.
(James, especially: col.5, lines 10 - col.6, line 12)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee '268 with those of James, because James (col.3, lines 22-30) expressly states that "A non-volatile device having a serial interface is described. Although the detailed description describes embodiments based on a flash memory device, the invention may be used in any non-volatile semiconductor memory, including, but not limited to EPROMs, EEPROMs, and flash memories, and including technologies such as NOR, NAND, AND, Divided bit-line (DINOR) and Ferro-electric random access memory (FRAM)." Lee '268 (see Abstract) teaches a "... novel nonvolatile Flash EEPROM array [that] preferably comprises a plurality of blocks which comprise a plurality of sectors of NOR-gate transistors."

32. In regards to Claim 21, Lee '268 teaches the following limitations:

> 21. The emulated EEPROM of claim 1 wherein the ratio of flash cells used to emulate one EEPROM memory cell is 8 to 1.
> (Lee '268, especially: col.3, line 62 – col.4, line 5)

33. In regards to Claim 22, Lee '268 teaches the following limitations:

> 22. AN emulated EEPROM memory array comprising:
>
> a NOR flash memory array located on an integrated circuit, the NOR flash memory array being organized into a plurality of sectors;
> (Lee '268, especially: col.3, line 62 – col.4, line 5)

However, Lee '268 does not expressly teach the following limitations. James, however, does teach these limitations:

> a microcontroller coupled for controlling data access to and from an addressing of the flash memory array,
> (James, especially: col.3, lines 22-30)
>
> an address counter whose output is coupled to an internal address bus of the memory array;
> (James, especially: Fig.2, Items 3,5,6,7,9; col.4, lines 4-14)
>
> a state machine coupled to the address counter and coupled for outputting control signals, the address counter receiving control signals from the state machine to control the loading of hard coded addresses in storage registers which are read and updated by the micro controller during a reset phase or by the state machine after an EEPROM update.
> (James, especially: Fig.2, Item 21; col.5, lines 10 - col.6, line 12)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Lee '268 with those of James, because James (col.3, lines 22-30) expressly states that "A non-volatile device having a serial interface is described. Although the detailed description describes embodiments based on a flash memory device, the invention may be used in any non-volatile semiconductor memory, including, but not limited to EPROMs, EEPROMs, and flash memories, and including technologies such as NOR,

NAND, AND, Divided bit-line (DINOR) and Ferro-electric random access memory (FRAM)." Lee '268 (see Abstract) teaches a "... novel nonvolatile Flash EEPROM array [that] preferably comprises a plurality of blocks which comprise a plurality of sectors of NOR-gate transistors."

34. In regards to Claim 24, Lee '268 teaches the following limitations:

> 24. An emulated EEPROM memory comprising:
> a NOR flash memory array positioned on an integrated circuit, the NOR flash structure being of a type that permits simultaneous erasing of all cells in an entire sector but does not permit simultaneous erasing of less than all cells in a sector, at least two of the sectors being structured to emulate an EEPROM having byte erasability, the byte comprising substantially few memory cells than an entire sector.
> (Lee '268, especially: col.2, line 45 –col.3, line 33; col.3, line 62 – col.4, line 5)

Response to Amendment

35. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

36. For example, Applicants argue (paper #15, p.9) that "This ELITE ARRAY [as taught in the Lee '923 patent] is part of the memory array itself and renders the FLASH array outside of NOR FLASH family." However, the limitation of "NOR Flash" only appears in Claims 22-24. Applicants argue (paper #15, p.9) that "Claim 1 has been amended to specify NOR FLASH array", yet Examiner does not see this limitation in the amended claim 1. Moreover, independent claims 8,

10, and 16, and their dependent claims have not been amended at all, and do not include this limitation. There is a typographical error in claim 1: "... memory cells Flash memory cells being emulated." Based on Applicants' arguments (paper #15, p.9), it appears that the intended limitation may have intended to claim "... NOR Flash memory cells being emulated." However, this does not currently appear in the claim.

37. Moreover, Applicants argue (paper #15, p.11) that "The present invention, on the other hand, uses software processing and a state machine in order to perform the emulation at the sacrifice of requiring the use of more NOR FLASH memory cells to emulate a few number of EEPROM cells. This concept is entirely missing from Lee '923 patent and, claim 1 is believed to be patentable as presently submitted." The limitations "software processing" and "a state machine" do not appear in claim 1, as asserted by the Applicants. These limitations appear only in claim 5.

38. In any case, Applicants' arguments regarding claims 1-5, 7, 21-22, and 24 are moot because new art has applied new art to reject these claims, as necessitated by amendment.

Allowable Subject Matter

39. Claims 6, 14-15, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

40. This action is non-final because new art has been applied to reject claims 8 and 10-20.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications: (703) 746-7239

Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

December 22, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER